



Non-Confidential Description
**Asynchronous Cellular Automaton Provides Benefits
Over Field-Programmable Gate Arrays**

Technology Case: RFT-256

Invention Summary

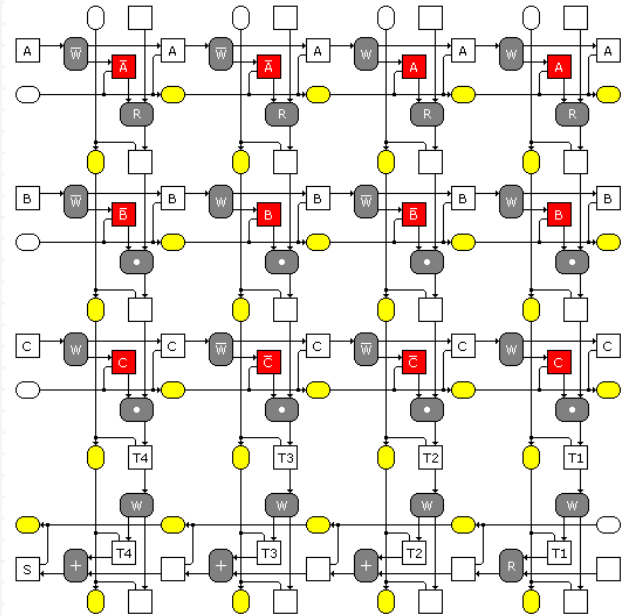
North Dakota State University scientists have created a unique asynchronous cellular automaton which is believed to have several distinct advantages over currently available field-programmable gate arrays (FPGAs) and similar computing devices. These cellular automata are easily scaled from small circuits to large computing arrays.

Benefits

- **Faster than FPGAs:** The cellular automata are driven by logic triggers – and therefore run at logic speed, not clock speed.
- **Lower power:** Individual cells only run when needed (when triggered), limiting the amount of power used.
- **Naturally scalable:** The cellular automata can be physically large. Because of their structure, they are easily extended without having to change the architecture of the chip.
- **Less expensive:** Because of the repeatable architecture, it is believed they will be cheaper than FPGAs when manufactured in quantity.
- **Thermally self-regulating:** Built in circuitry controls rate of computation to prevent overheating.

Invention Premise

The present invention is an initial version of a cellular automaton (CA) in which computation is driven by triggers instead of by a clock signal. A trigger is a single pulse that is generated within and used by a cell. A trigger usually signifies the arrival of a bit of data. Upon receipt of a trigger, the receiving cell generates a new pulse, thus ensuring the integrity (in particular, the duration) of the pulse. The circuitry that generates the trigger is called a trigger generator. The trigger generator delays the production of the new pulse until the circuitry within the cell has had sufficient time to process the input data bit and produce a result. The new pulse is used to latch the result and to trigger an adjacent cell. Triggers are cell-to-cell events by which cellular computations are initiated. A computation in a CA proceeds along paths of cascaded trigger events.



Example of the technology. A 1-bit adder with carry input created with an array of quad cells.

Patents

This technology is patent pending with world-wide rights preserved and immediately available for licensing/partnering opportunities.

The Inventor



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Dr. Mark Pavicic received a Bachelor of Science in both Electrical Engineering and Physics/Mathematics in 1974 from Iowa State University. He then earned an Master of Science in Electrical Engineering in 1976 from the University of Illinois, and in 1985 received a M.Ph. and Ph.D. in Electrical Engineering from Columbia University.

Before coming to the Center for Nanoscale Science and Engineering (CNSE) in 2006, Pavicic began his career at Texas Instruments and moved on to hold positions at IBM, North Dakota State University (NDSU), Microsoft, and Dakota Technologies. During his years at Texas Instruments and IBM, he received three U.S. patents for his work on processors and computer displays. He was the primary designer on Texas Instruments' TMS32010 Digital Signal Processor, a chip that was recently listed in the IEEE article entitled "**25 Microchips That Shook the World**". He later received three more patents while working with digitizing chips at Dakota Technologies. While at NDSU, Pavicic became an Associate Professor in the Computer Science department and taught a broad range of subjects.

Pavicic joined CNSE as a Senior Research Scientist in 2006. He is currently the NDSU Principal Investigator for the Conformal Computing Program, a collaboration sponsored by the Department of Defense between NDSU and MIT to investigate a new computational paradigm.

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